I CLAIM:

1. A method of modeling a semiconductor device comprising the steps of:

a) modeling a small signal electrical equivalent circuit for said semi conductor which includes a plurality of electrical circuit elements defining a small signal model;

b) deriving said electrical circuit elements from a small signal excitation analysis of one or more predetermined characteristics of said semiconductor device.

2. The method as recited in claim 1, wherein step (b) includes deriving the electrical circuit elements from a small signal excitation analysis of the intrinsic charge within the semiconductor device.

3. The method as recited in claim 2, wherein step (b) further includes deriving the electrical circuit elements from a small signal excitation analysis of the electric fields within the device

4. The method as recited in claim 1, wherein step (b) further includes deriving the electrical circuit element from a small signal excitation analysis of the electric fields within the device.

5. The method as recited in claim 2, wherein step (b) includes the following step:

d) determining the relationships between one or more the conduction band offsets and electrical permitivities and the material composition for the materials in the semiconductor.

6. The method as recited in claim 5, wherein step (d) is determined analytically.

7. The method as recited in claim 6, wherein step (d) is determined by fitting simulated data.

8. The method as recited in claim 5, further including step (e); determining the electron transport characteristics of any bulk materials in the semiconductor.

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~~9. The method as recited in claim 8, further including step (f); determining the undepleted linear channel mobility.~~

~~10. The method as recited in claim 9, wherein step (b) is determined by material characterization.~~

11. The method as recited in claim 9, wherein step (f) is determined by physical simulation.

12. The method as recited in claim 9, further including step (g) determining the Schottky barrier height expressions.

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~~13. The method as recited in claim 12, further including step (h) forming semi-physical equations with empirical terms for modeling one or more of the following characteristics: fundamental-charge control physics for sheet charge in the active channel as controlled by the gate terminal voltage; average centroid position of the sheet charge within the active channel width; position of charge partitioning boundaries as a function of gate, drain and source terminal voltages; bias dependence of linear channel mobility and surface depleted regions; bias dependence of the velocity saturating electric field of the channel; saturated electron velocity; electrical conductance within the linear region of the channel, under the gate; electrical conductance within the source and drain access regions.~~

14. The method as recited in claim 13, further including step (i):

adjusting the empirical terms of the semi-physical equations to fit the model current-voltage (I-V) characteristics relative to measured values.

15. The method as recited in claim 14, further including steps (j):

iteratively readjusting the empirical terms to achieve a simultaneous fit of measured capacitance voltage (C-V) and I-V characteristics.

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